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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,569	09/29/2000	Ravi P. Singh	10559/292001/P9299-ADI	3025

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EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/675,569	SINGH ET AL.
	Examiner	Art Unit
	Midys Inoa	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on October 25th, 2002 has been considered by the examiner.

Drawings

2. The drawings filed on September 29th, 2000 have been accepted by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims18-23 and 27-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Bachand et al. (US 2003/0115424).

Regarding Claims 18, 20, 27 and 29, Bachand et al discloses setting a least significant bit ("blocking bit") of a branch target address ("new transaction") in response to a new address pair matching a stored address pair (comparing the new address pair, Page 3, paragraph 0038). The stored address pair is stored in both cache 220 and in a first pair of registers ("the internal transaction queue 230").

Regarding Claims 22 and 31, Bachand et al. discloses comparing the new address pair to the stored address pairs in order to determine if the new address pair matches any of the stored address pairs; therefore the new address pair must be compared to all the stored address pairs in the system (first, second, third, etc). Bachand also discloses setting a least significant bit

("blocking bit") of a branch target address ("new transaction") in response to the new address pair matching any stored address pair (Page 3, paragraph 0038), and not blocking the new transaction if it does not match a previous transaction. If it is not blocked, the new transaction will eventually be passed to cache 220 and stored in the internal transaction queue 230 (Page 3, paragraph 0038 – 0041)

Regarding Claims 19, 23, 28, and 32 Bachand et al. discloses blocking the new transaction (new address pair) in response to the new transaction matching the stored previous transactions. In this case, blocking the transaction is analogous to discarding the transaction since it becomes blocked from usage.

Regarding Claims 21 and 30, Bachand et al. discloses not blocking the new transaction if it does not match a previous transaction. So, the new transaction will eventually be passed to cache 220 and stored in the internal transaction queue 230 (Page 3, paragraph 0038 – 0041)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7, 12-17, and 24-26, are rejected under 35 U.S.C. 103(a) as being unpatentable over Panigrahi (3,975,717).

Regarding Claim 1, Panagrahi discloses a stack comprising a plurality of interconnected registers (R11-R52), including a first end register R11 to input and output instruction addresses,

a second end register R52, and a plurality of middle registers connected between said first end registers and said second end register (R12 – R51); and a write path coming from push circuit 19 to shift an instruction address in one of said plurality of interconnected registers by one register pair toward the second end register on a write operation (see Figure 1A and Column 5, lines 28-49). Panagrahi does not teach shifting the instruction address by two registers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Panagrahi so that the input bus has double the width supported by the registers in the stack in order to allow the system to transfer more data into the stack in less time. In the case where this input bus where to be implemented, the system would have to push an input from such input bus into the stack by shifting the input by two register pairs in order to accommodate one input of double the size of one register pair.

Regarding Claim 13, Panagrahi discloses a stack comprising a plurality of interconnected registers (R11-R52), including a first end register R11 to input and output instruction addresses, a second end register R52, and a plurality of middle registers connected between said first end register and said second end register (R12 – R51); and a write path coming from push circuit 19 to shift a instruction address in one of said plurality of interconnected registers by one register pair toward the second end register on a write operation (see Figure 1A and Column 5, lines 28-49) and a read path coming from pop circuit 12 to shift a instruction address by one register toward the first end register on a read operation (Column 4, line 67 – Column 5, line 16). Panagrahi does not teach shifting the instruction address by two registers in a write operation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Panagrahi so that the input bus has double the width supported by the

registers in the stack in order to allow the system to transfer more data into the stack in less time. In the case where this input bus where to be implemented, the system would have to push an input from such input bus into the stack by shifting the input by two register pairs in order to accommodate one input of double the size of one register pair.

Regarding Claim 2, Panagrahi discloses a stack comprising a read path coming from pop circuit 12 to shift an instruction address by one register toward the first end register on a read operation (Column 4, line 67 – Column 5, line 16).

Regarding Claims 3 and 14, Panagrahi discloses a stack, which operates as a first-first-out (FIFO) register on the write operation and as a last-in-first-out (LIFO) register on the read operation. The system of Panagrahi is capable of both LIFO and FIFO operations and selectively enables read and write operations at either LIFO or FIFO modes (see Abstract).

Regarding Claims 4-5, and 15-16, Panagrahi discloses a stack in which each register pair has the capacity to take in an input the size of a 2n bit word (Column 3, lines 59-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the size of each register and the size of each input (instruction address) 32-bits wide since this is a common word size and it allows for faster transmission rates as opposed to smaller word sizes (i.e. 16-bit words).

Regarding Claim 6, Panagrahi discloses a stack system comprising a plurality of registers 1 through M, where M is not defined. It is understood that M could be 32, thus making the total number of registers 32.

Regarding Claims 7 and 17, Panagrahi discloses a stack system with a 2n-bit bus to read a 2n-bit instruction address from the first end register on the read operation where n can be equal

to 16 (Column 4, line 67 – Column 5, line 16). Panagrahi does not teach a 64-bit write bus to write a 64-bit address pair to the first end register and an adjacent register on the write operation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Panagrahi so that the input bus has double the width supported by the registers in the stack (64-bits) in order to allow the system to transfer more data into the stack in less time. In the case where this input bus where to be implemented, the system would have to push an input from such input bus into the stack by shifting the input by two register pairs in order to accommodate one input of double the size of one register pair.

Regarding Claim 12 Panagrahi discloses a stack comprising a plurality of interconnected flip-flops (R11-R52), including a first end flip-flop R11 to input and output valid bits, a second end flip-flop R52, and a plurality of middle flip-flops connected between said first end flip-flop and said second end flip-flop (R12 – R51); and a write path coming from push circuit 19 to shift a valid bit in one of said plurality of interconnected flip-flops by one flip-flop pair toward the second end flip-flop on a write operation (see Figure 1A and Column 5, lines 28-49) and a read path coming from pop circuit 12 to shift a valid bit by one flip-flop toward the first end flip-flop on a read operation (Column 4, line 67 – Column 5, line 16). Panagrahi does not teach shifting the valid bit by two registers in a write operation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Panagrahi so that the input bus has double the width supported by the flip-flops in the stack in order to allow the system to transfer more data into the stack in less time. In the case where this input bus where to be implemented, the system would have to push an input from such input bus

into the stack by shifting the input by two flip-flop pairs in order to accommodate one input of double the size of one flip-flop pair.

Regarding Claim 24, Panagrahi discloses a stack, which operates as a first-first-out (FIFO) register on the write operation and as a last-in-first-out (LIFO) register on the read operation. The system of Panagrahi is capable of both LIFO and FIFO operations and selectively enables read and write operations at either LIFO or FIFO modes (see Abstract). The stack system of Panagrahi has a 2n-bit bus to read a 2n-bit instruction address from the first end register on the read operation where n can be equal to 16, thus making the read bus 32-bit wide (n-bit wide, Column 4, line 67 – Column 5, line 16). Panagrahi does not teach a 64-bit (2n) write bus to write a 64-bit address pair to the first end register and an adjacent register on the write operation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Panagrahi so that the input bus has double the width supported by the registers in the stack (64-bits) in order to allow the system to transfer more data into the stack in less time.

Regarding Claim 25, Panagrahi discloses a stack comprising register pairs with the capacity to take in an input the size of a 2n bit word (Column 3, lines 59-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the size of each register and the size of each input (instruction address) 32-bits wide since this is a common word size and it allows for faster transmission rates as opposed to smaller word sizes (i.e. 16-bit words).

Regarding Claim 26, an address pair usually comprises information identifying the targeted information (target address, i.e. location) and information regarding the nature of the access request (source address).

7. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panigrahi (3,975,717) in view of Bachand et al. (US 2003/0115424 A1).

Regarding Claims 8-9, Panigrahi discloses the invention as set forth by claim 1 above. Panigrahi does not teach a first and second holding register, a first and second comparator, and a compression indication circuit to generate an indicator in response to a new input matching stored data. Bachand et al. discloses a snoop queue 250 ("first holding registers"), an external transaction queue 240 ("second holding register"), an observation transaction logic ("first/second comparator") to compare the address of the new transaction with addresses of earlier-posted transactions, and a control logic 254 ("compression indication circuit") to enable the blocking bit, which could be the least significant bit, of the new transaction in response to a match signal (Page 3, paragraphs 0037 – 0038). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the comparison and blocking operations of Bachand et al. with the system of Panigrahi because doing so would give the system coherency capabilities and thus allow the stack of Panigrahi to avoid storing redundant data.

Regarding Claims 10-11, in the invention of Panigrahi in view of Bachand et al., the stack of Panigrahi would hold the previously posted transactions. Being that the stack is composed of many registers ("second/third adjacent registers") and the observation transaction logic is to compare the new transaction with previously posted transactions, the observation transaction logic would act as a comparator for each register of the stack ("third and fourth

comparators"). The control logic 254 ("compression indication circuit") then enables the blocking bit of the new transaction, which could be a least significant bit, in response to a match signal if a match is detected (Page 3, paragraphs 0037 – 0038).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa
Examiner
Art Unit 2188

MI

GARY PORTKA
PRIMARY EXAMINER